



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,209	07/19/2005	Takashi Aoyama	TIC-0085	8779
23377	7590	04/30/2008	EXAMINER	
WOODCOCK WASHBURN LLP			PUENTE, EVA YI ZHENG	
CIRA CENTRE, 12TH FLOOR				
2929 ARCH STREET			ART UNIT	PAPER NUMBER
PHILADELPHIA, PA 19104-2891			2611	
			MAIL DATE	DELIVERY MODE
			04/30/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/523,209	AOYAMA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	EVA Y. PUENTE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 25 July 2003.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-7 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1 and 4-6 is/are rejected.  
 7) Claim(s) 2,3 and 7 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 25 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>9/9/05</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

### ***Drawings***

1. Figures 1A, 1B, and 1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

2. Claim 6 is objected to because of the following informalities:

- (a) on line 3, please change "a" and add -- the -- before "phase".
- (b) on line 4, please delete "a" and add -- said -- before "base".
- (c) on line 12, please delete "a" and add -- the -- before "phase".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being unpatentable by Sashida

(US 5,422,518).

a) Regarding claim 1, a digital VCO (14 in Fig. 10) comprising:  
a quartz oscillation circuit generating a signal having a predefined frequency by using a quartz oscillator (21; Col 2, L48-58);  
a conversion circuit converting a given analog signal to a digital signal (23); and  
a divider circuit dividing a frequency of signal generated in said quartz oscillation circuit by a division ratio according to said digital signal (22, 24 and 25).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida (US 5,422,518) in view of Rudberg (US 6,351,227).

Regarding claim 4, Sashida discloses a digital VCO comprises an analog to digital converter (23 in Fig. 10) and all the subject matters described above except for the specific teaching of a compensation circuit.

However, Rudberg disclose an A/D conversion offset error correction system (Fig. 5), wherein comprise a A/D (10) and an offset correction unit (14) for compensating an offset error of the digital signal occurred in the A/D (Col 3, L31-52). The offset error estimation is repeated periodically to compensate for slow changes in the offset error of D/A converter, i.e. temperature changes (Col 3, L52-54). Therefore, it is obvious to one of ordinary skill in the art to apply the A/D error compensation teaching of Rudberg with the A/D conversion of Sashida. By doing so, improve A/D conversion accuracy and reduce power consumption in a digital communication system.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida (US 5,422,518) in view of Fowks (US 4,446,446).

Regarding claim 5, Sashida discloses a digital VCO and all the subject matters described above except for the specific teaching of a frequency division ratio limiting circuit.

However, Fowks discloses a variable frequency synthesizer system (Fig. 2), wherein comprise a crystal oscillator (22), applied to a programmable divider (32), which is connected to a phase comparator (34). The programmable divider is also control by a 8-bit binary code through bus 33. The division ratio may be any number from 0 to 255 (Col 6, L50 - Col 7, L3). Therefore, it is obvious to one of ordinary skill in the art to substitute the programmable divider teaching of Fowks for the conventional frequency divider of Sashida. By doing so provide precise frequency control (Col 13, L54-60).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lilley et al (US 4,819,196) in view of Sashida (US 5,422,518).

a) Regarding to claim 6, Lilley et al disclose a PLL circuit adjusting a phase difference between input signal and a base signal (Fig. 1), including:

a detection circuit detecting a phase difference between said input signal and a base signal (16); and

a quartz oscillation circuit generating a signal having a predefined frequency by using a quartz oscillator (20 is a crystal VCO; Col 6,L 20-21).

Lilley et al did not explicitly show the details of the crystal VCO. However, Sashida discloses a digital VCO (14 in Fig. 10) comprising: a quartz oscillation circuit generating a signal having a predefined frequency by using a quartz oscillator (21; Col 2, L48-58); a conversion circuit converting a given analog signal to a digital signal (23); and a divider circuit dividing a frequency of signal generated in said quartz oscillation circuit by a division ratio according to said digital signal (22 and 24). Another frequency divider (25) is coupled to the output of the digital VCO. A quartz oscillator (crystal oscillator) is a well known device for creating precise frequency in digital integrated circuits. By implementing the digital VCO as taught by Sashida in the phase control system of Lilley et al., the phase difference between the input signal and the base signal is adjusted according to the divided frequency. Therefore, it is obvious to one of ordinary skill in the art to combine the digital VCO as taught by Sashida with the phase control system of Lilley et al. By doing so, provide stable clock signal, and optimal phase track and adjustment.

***Allowable Subject Matter***

9. Claims 2, 3, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Puente whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Puente  
/E. Y. P./  
Examiner, Art Unit 2611

April 17, 2008

/Chieh M Fan/  
Supervisory Patent Examiner, Art Unit 2611